first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively,

wherein the first and second main pump capacitors are prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level is moves to a third predetermined level in response to the plurality of phase generators during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively.

26. (Twice Amended) A memory device, comprising:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors coupled [between the first and second main pump capacitors and] to the first and second preboot capacitors; and

first and second gating devices coupled to the first and second main pump capacitors, respectively.

28. (Twice Amended) A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit comprises at least one memory device, further wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors coupled [between the first and second main pump capacitors and] to the first and second preboot capacitors; and

first and second gating devices coupled to the first and second main pump capacitors, respectively.

29. (Twice Amended) A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit comprises at least one memory device, further wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors coupled [between the first and second main pump capacitors and] to the first and second preboot capacitors; and

first and second gating devices coupled to the first and second main pump capacitors, respectively.

31. (Twice Amended) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors coupled [between the first and second main pump capacitors and] to the first and second preboot capacitors; and

first and second gating devices coupled to the first and second main pump capacitors, respectively.

33. (Twice Amended) An electronic system, comprising:

a processor; and

at least one memory device coupled to the processor, wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors coupled [between the first and second main pump capacitors and] to the first and second preboot capacitors; and

first and second gating devices coupled to the first and second main pump capacitors, respectively.

42. (New) The charge pump of claim1, further comprising:

first and second sharing transistors coupled to the first and second pre-boot pre-charge capacitors and the first and second pre-boot capacitors to provide a path that charge shares the first and second pre-boot capacitors to the first and second main pump capacitors.